WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate having a well of a first conduction type;

an impurity region of a second conduction type disposed in the well;

a lower interlayer dielectric stacked on the substrate including the well and the impurity region;

a contact plug connected to the impurity region through the lower interlayer dielectric;

an upper interlayer dielectric formed on the lower interlayer dielectric including the contact plug;

an interconnection connected to the contact plug through the upper interlayer dielectric; and

a seam formed below the contact plug and connected to the well.

2. The semiconductor device of claim 1, wherein the well of the first conductive type is an N-well to which a well bias of a power supply voltage can be applied through the seam.

3. The semiconductor device of claim 2, wherein the impurity region of the second conduction type is a source region of a pull-up transistor in an SRAM cell, and the interconnection is a power supply line.

4. The semiconductor device of claim 1, wherein the well of the first conduction type is a P-well to which a well bias of a ground voltage can be applied through the seam.

5. The semiconductor device of claim 4, wherein the impurity region of the second conduction type is a source region of a driver transistor in an SRAM cell, and the interconnection is a ground line.

6. The semiconductor device of claim 1, wherein the contact plug and the interconnection are made of tungsten (W).

7. A semiconductor device comprising:

a substrate where a well of a first conduction type is formed;

a first impurity region and a second impurity region of a second conduction type formed in the well of the first conduction type, the first and second impurity regions being spaced apart from each other;

a lower interlayer dielectric formed on the substrate including the first and second impurity regions;

a first contact plug electrically connected to the first impurity region through the lower interlayer dielectric;

a second contact plug electrically connected to the second impurity region through the lower interlayer dielectric;

an upper interlayer dielectric formed on the lower interlayer dielectric including the first and second contact plugs; and

a first interconnection connected to the first contact plug through the upper interlayer dielectric and a second interconnection connected to the second contact plug through the upper interlayer dielectric, wherein the second contact plug is wider than the first contact plug and wherein a seam is formed below the second contact plug that is coupled to the well.

8. The semiconductor device of claim 7, wherein a well bias can be applied through the seam connecting the second contact plug to the well.

9. The semiconductor device of claim 7, wherein the first conduction type is an N-type.

10. The semiconductor device of claim 9, wherein a power supply voltage can be applied to the second interconnection and the second contact plug.

11. The semiconductor device of claim 7, wherein the first conduction type is a P-type.

12. The semiconductor device of claim 11, wherein a ground voltage can be applied to the second interconnection and the second contact plug.

13. The semiconductor device of claim 7, wherein the first and second contact plugs are made of tungsten (W).

14. The semiconductor device of claim 7, wherein the second impurity region is a source region of a driver transistor in an SRAM cell and the second interconnection is a ground line.

15. The semiconductor device of claim 7, wherein the second impurity region is a source region of a pull-up transistor in an SRAM cell and the second interconnection is a power supply line.

16. A method of fabricating a semiconductor device, comprising:

forming a well of a first conduction type in a substrate;

forming an impurity region of a second conduction type in the first conduction type well;

forming a lower interlayer dielectric on the substrate including the well and the impurity region;

selectively etching the lower interlayer dielectric to form an opening exposing the impurity region;

filling the opening with a first conductive layer to form a contact plug, wherein a void is formed in the contact plug;

forming an upper interlayer dielectric on the lower interlayer dielectric including the contact plug;

selectively etching the upper interlayer dielectric to form an interconnection groove exposing the contact plug;

overetching the contact plug and a substrate including the exposed void to expose the void to the well; and

filling the interconnection groove with a second conductive layer to form an interconnection, wherein a seam connecting the contact plug to the well is formed at the void extended to the well.

17. A method of fabricating a semiconductor device, comprising:

forming a well of a first conduction type in a substrate;

forming a first impurity region and a second impurity region of a second conduction type in the first conduction type well, the first and second impurity regions being spaced apart from each other;

forming a lower interlayer dielectric on the substrate having the first conduction type well and the impurity region of the second conduction type;

selectively etching the lower interlayer dielectric to form a first opening exposing the first impurity region and a second opening exposing the second impurity region, the second opening being wider than the first opening;

filling the first and second openings with a first conductive layer to form a first contact plug and a second contact plug, wherein a void is formed in the second contact plug;

forming an upper interlayer dielectric on a lower interlayer dielectric including the first and second contact plugs;

selectively etching the upper interlayer dielectric to form a first interconnection groove and a second interconnection groove;

overetching the second contact plug exposed below the second interconnection groove to extend the void to the first conduction type well; and

filling the first interconnection groove with a second conductive layer to form a first interconnection; and

filling the second interconnection groove and filling the void by forming a seam connecting the contact plug to the well.

18. A method of fabricating a semiconductor device comprising:

forming a well of a first conduction type in a substrate;

forming an impurity region of a second conduction type in the well;

forming a lower dielectric layer over the substrate, the well, and the impurity region;

forming a contact plug that connects to the impurity region through the lower dielectric layer, the contact plug having a void with an opening at a top of the contact plug that extends into the contact plug;

extending the void through the impurity region and into the well by overetching the contact plug; and

filling the void with a conductive layer.

19. The method of claim 18, where the contact plug and the conductive layer are both composed of tungsten (W).